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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,305	09/24/2003	Al Fang	5646-103	3134

20792 7590 04/04/2005

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,305	FANG ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04, 8/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of claims 9 and 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 9-10, 14-15, 22-23 and 27-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin (USP 2004/0158757).

Figure 9 shows a delay locked loop comprising a phase interpolator circuit (99) and a variable delay circuit (96) coupled in cascade and operative to generate to output clock signal (CLKOUT) that is delayed with respect to a reference clock signal responsive to respective first and second control signals (outputs of 95, 98) applied to the phase interpolator and the variable delay circuit, and a phase control circuit (95, 98) that generates the first and second control signals responsive to the output clock signal and the reference clock signal as called for in claims 1, 14 and 27.

Regarding claim 2, the variable delay circuit provides a coarser resolution than the phase interpolator circuit.

Regarding claim 3, the variable delay circuit is configured to provide step changes in delay responsive to the second control signal (output of 95).

Regarding claim 9, the variable delay receives the reference clock and the phase interpolator receives output of the variable delay circuit.

Regarding claim 10, the phase detector and delay control block are seen as the phase detectors and control blocks 95 and 98 of figure 9.

Regarding claims 15, 23 and 28, the phase interpolator provide fine delay adjustment and the variable delay circuit provide a coarse delay adjustment.

Regarding claim 22, the variable delay circuit precedes the phase interpolator.

3. Claims 1-3, 8, 10, 14-15, 21, 23 and 27-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (USP 6,836,166).

Figure 2 shows a delay locked loop comprising a phase interpolator circuit (210 fine delay line) and a variable delay circuit (216 coarse delay line) coupled in cascade and operative to generate to output clock signal (CLKDEL) that is delayed with respect to a reference clock signal (CLK) responsive to respective first and second control signals (FS, BCS) applied to the phase interpolator and the variable delay circuit, and a phase control circuit (228, 214) that generates the first and second control signals responsive to the output clock signal and the reference clock signal as called for in claims 1, 14 and 27.

Regarding claims 2, 15 and 28, the variable delay circuit provides a coarser resolution than the phase interpolator circuit.

Regarding claim 3, the variable delay circuit is configured to provide step changes in delay responsive to the second control signal.

Regarding claims 8 and 21, the phase interpolator precedes the variable delay circuit.

Regarding claims 10 and 23, figure 2 shows a phase detector 228, a delay control circuit (214).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 9-10, 14-18, 20, 22-23 and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller, Jr. (USP 6,281,726).

Figure 3 shows a delay locked loop comprising a phase interpolator circuit (50) and a variable delay circuit (42, 46) coupled in cascade and operative to generate to output clock signal (CLKOUT) that is delayed with respect to a reference clock signal (CLKIN) responsive to respective first and second control signals (outputs of 44, 54) applied to the phase interpolator and the variable delay circuit, and a phase control circuit (48) that generates the first and second control signals responsive to the output clock signal and the reference clock signal as called for in claims 1, 14 and 27.

Regarding claim 2, the variable delay circuit provides a coarser resolution than the phase interpolator circuit.

Regarding claim 3, the variable delay circuit is configured to provide step changes in delay responsive to the second control signal (output of 44).

Regarding claims 4 and 16, the variable delay comprising a plurality delay circuits (providing a plurality delay signals (D1-Dz) interconnected by a switching circuit (z to 1 mux) that is operative to selectively bypass one or more delay circuits responsive to the second control signal.

Regarding claims 5 and 18, the phase control circuit (counters 44 and 54) is operative to cause the phase interpolator circuit to shift from one extreme of a delay range (from 1) thereof towards another extreme of the delay range (Z) concurrent with a step change in delay through the variable delay circuit (the delay circuit is also controlled by the same 1 to z counter size).

Regarding claim 9, the variable delay receives the reference clock and the phase interpolator receives output of the variable delay circuit.

Regarding claims 10 and 23, the phase detector and delay control block are seen as the phase detectors and control blocks 44, 54 of figure 3.

Regarding claims 15 and 28, the phase interpolator provide fine delay adjustment and the variable delay circuit provide a coarse delay adjustment.

Regarding claim 17, the recited limitations are seen inherently present in figure 3 of Saitoh et al.

Regarding claims 7 and 20, figure 4 shows an analog phase interpolator.

Regarding claim 22, the variable delay circuit precedes the phase interpolator.

5. Claims 1-7, 9-20 and 22-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitoh et al. (SP 5,604,775).

Figure 3 shows a delay locked loop comprising a phase interpolator circuit (fine stepsize delay 13) and a variable delay circuit (coarse stepsize delay 11) coupled in cascade and operative to generate to output clock signal (output of clock tree) that is delayed with respect to a reference clock signal (Reference clock) responsive to respective first and second control signals (X0-X6, Y0-Y2) applied to the phase interpolator and the variable delay circuit, and a phase control circuit (phase detector 30, delay controller 40) that generates the first and second control signals responsive to the output clock signal and the reference clock signal as called for in claims 1, 14 and 27.

Regarding claim 2, the variable delay circuit provides a coarser resolution than the phase interpolator circuit.

Regarding claim 3, the variable delay circuit is configured to provide step changes in delay responsive to the second control signal (X0-X6).

Regarding claims 4 and 16, the variable delay comprising a plurality delay circuits (providing a plurality delay signals interconnected by a switching circuit (selector 115) that is operative to selectively bypass one or more delay circuits responsive to the second control signal.

Regarding claims 5 and 18, the phase control circuit is operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the variable delay circuit (selector of the coarse delay circuit is 3 bit control selector (X0-X2), the fine delay circuit is also a 3 bits control delay circuit (Y0-Y2), thus, the step changes in the fine delay circuit is concurrent with step change in the variable delay circuit).

Regarding claims 6, 19, figure 6 shows a fine delay circuit having the first and second delay circuits (121, 122) coupled in series and generating respective first and second delayed clock signals, and a phase interpolator (120-1) receives the first and second delayed clock circuit and that generates a phase interpolated clock signal therefrom.

Regarding claims 7 and 20, figure 6 shows an analog phase interpolator.

Regarding claim 9, the variable delay receives the reference clock and the phase interpolator receives output of the variable delay circuit.

Regarding claims 10 and 23, the phase detector and delay control block are seen as the phase detectors and control blocks 30 and 40 of figure 3.

Regarding claims 11 and 24, figure 10 shows the delay control circuit comprises a fine control counter circuit (460) that increment and decrements a fine control signal (Z0-Z2) in

response to the error signal (U/D) and that generates a count limit indicator (C/B) responsive to the fine control count signal reaching one of maximum or minimum count (carry output is at logic one when it is a full count), and a coarse control counter circuit (461) that increments and decrements a coarse control count signals (Z3-Z4) responsive to the error signal (U/D) subject to the count limit indicator signal (counter 461 is enabled when both C/B and the enable signal EN1 are at logic high), wherein the phase interpolator circuit is responsive to the fine control count signal and the variable circuit is responsive to the coarse control count signal.

Regarding claims 12 and 25, the coarse control counter circuit is enabled to count responsive to assertion of the count limit indicator (counter 461 is enabled when both C/B and the enable signal EN1 are at logic high).

Regarding claims 13 and 26, the first and second error signals are the Up and Down output signals of the phase detector, the fine control counter circuit (460 of figure 10) increments or decrements responsive to one of the first and second error signals, and wherein the coarse control counter circuit (461 of figure 10) increments and decrements responsive to respective ones of the first and second error signals.

Regarding claims 15 and 28, the phase interpolator provide fine delay adjustment and the variable delay circuit provide a coarse delay adjustment.

Regarding claim 17, the recited limitations are seen inherently present in figure 3 of Saitoh et al.

Regarding claim 22, the variable delay circuit precedes the phase interpolator.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

3/30/2005